Zilog

Application note

Z80-CPU Systems Design Series

Interfacing 16 Pin Dynamic RAMs to the Z80A™ Microprocessor

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INTERFACING 16 PIN DYNAMIC RAMS TO THE Z80A MICROPROCESSOR

This application note will present the major design considerations and a design example for interfacing the 16 pin dynamic RAM devices, both 4K and 16K, to the Z80 and Z80A microprocessors. These devices will be emphasized because they are fast becoming the favorite memory component for data storage in microprocessor based systems. The 16K RAM (Zilog 6116) in particular, with design improvements over the 4K devices, will substantially reduce memory cost by quadrupling memory density in a package that is pin compatible with the 4K RAM.

This application note assumes a basic understanding of the Z80A CPU and dynamic RAM elements. The reader is referred to selected specification sheets on the various 4K and 16K dynamic RAMS and to the following Zilog literature:

Z80A CPU Technical Manual

Z6116 16K Dynamic RAM Product Specification

INTRODUCTION

Dynamic RAM Interface is greatly simplified using the Z80A microprocessor. During each memory opcode fetch cycle a dedicated line from the CPU ($\overline{RFSH}$), is used to indicate that a refresh read of all dynamic memories should be performed. With $\overline{RFSH}$ in the true state (LOW), the lower 7 bits of the address bus identify one ROW address to be refreshed. Before the next opcode fetch, this address will have been incremented to point to the next ROW address. Since it is only necessary to refresh the 'ROWS', a total of 64 refresh cycles will refresh an entire 4K RAM, or 128 refresh cycles for a 16K RAM. Z80A-CPU refreshing is automatically performed during a portion of the instruction fetch cycle which is used for internal processing. Thus the effect of refreshing the RAM is totally transparent to program execution, preventing the necessity of stealing cycles or stopping the CPU as would otherwise be required.

16 PIN DYNAMIC RAM ADDRESSING

To select a unique bit location, the 4K RAM element will require 12 address lines while the 16K device requires 14. For the 16 pin RAM device to accomodate these lines, it will be required to divide then into two groups; Row addresses and Column addresses (6 each for the 4K RAM and 7 each for the 16K RAM). Each group is applied to the RAM on the same input lines through an external multiplexer and latched into the chip by applying two clock strobes in succession. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the Row address bits into the RAM (A0-A5 for the 4K, A0-A6 for the 16K). The second clock, the Column Address Strobe ($\overline{CAS}$), latches the Column address bits, (A6-A11 for the 4K, A7-A13 for the 16K) into the RAM.

$\overline{RAS}$ activates one of the 64 Rows in the 4K device or one of 128 Rows in the 16K device. All memory locations in the selected Row are gated to sense amplifiers where each cell's logic level is discriminated, latched and rewritten.

$\overline{CAS}$ activates the Column decoder which selects 1 of 64 or 128 sense amplifiers and gates the selected cell from the Row Column Matrix to the output buffer.

During refresh the interface logic will enable the Row Address lines from the multiplexer. The CPU with a true condition on the Refresh line ($\overline{RFSH}$) will then present the address (A0-A7) of the Row to be refreshed.

MEMORY REFRESH

When any row in a 16 pin dynamic RAM is actively cycled, all locations within that row are refreshed. To refresh the entire RAM it is only necessary to perform a $\overline{RAS}$ only memory cycle ($\overline{CAS}$ is not required for a refresh sequence) at each of the 64 row addresses for the 4K device and 128 row addresses for the 16K device, every 2 milliseconds or less.

The Z80 CPU refreshes the memory more frequently than is necessary to meet the 2 ms row refresh requirement. Under worst case conditions, no more than 19T states will separate opcode fetch cycles (the EX (SP),HL instruction is representative of the longest time between opcode fetches). Assuming this worst case period between opcode fetches and, therefore, refresh cycles, the following times for total refresh for both 4K and 16K RAMS at 2.5 MHZ and 4 MHZ are shown below:

REFRESH TIME			
MEMORY SIZE	Z80-CPU @2.5 MHZ	Z80A-CPU @4.0 MHZ	NO. OF REQUIRED REFRESH CYCLES/2 mS
4K	487 us (max)	304 us (max)	64
16K	958 us (max)	608 us (max)	128

TABLE 1 WORST CASE MEMORY REFRESH CYCLES ASSUMING NO WAIT STATES

From the above table, it can be seen that the worst case refresh time for 16K RAMS consumes approximately 1/2 of the available 2 ms time interval while the 4K RAM consumes only about 1/4 of the allotted time. This provides for optional use of the refresh cycle for other CPU transparent bus activity such as DMA and CRT refresh.

ACCESS TIME

Most dynamic RAMS have access times in the range of 150 to 300 ns. This access begins with the leading edge of the row address strobe ($\overline{RAS}$). The column address strobe ($\overline{CAS}$) completes this access cycle. The time between the fall of $\overline{RAS}$ and the fall of $\overline{CAS}$ is identified as the $\overline{RAS}$ to $\overline{CAS}$ delay time (tRCD), and can be related to the previous access times as follows:

tRACmax = tRCDmax + tCACmax

WHERE tRACmax = Access time from RAS

tRCDmax = max RAS to CAS delay time

tCACmax = Access time from CAS

As long as tRCD is less than max value, (but greater than tRCDmin), the worst case access is from $\overline{RAS}$ (See Figure 1). If $\overline{CAS}$ is applied at a point in time beyond the tRCDmax limit, the access time from $\overline{RAS}$ will be lengthened by the amount that tRCD exceeds the tRCDmax limit and the access time from $\overline{CAS}$ (tCAC) will be the critical parameter. Note, however, that reducing tRCD to something less than tRCDmax will have no effect at reducing tRACmax.

The significance of the min/max value on tRCD is that $\overline{CAS}$ can be brought low any time within this window and not affect access time. This is a great improvement from early 4K designs that required $\overline{CAS}$ to be brought low at a set minimum time from $\overline{RAS}$ low in order to avoid increasing access time. This made no allowance for the time required to switch the MUX from ROW to COLUMN addresses, requiring that the worst case multiplexing time delay to be added to the specified access time.

This window for the application of the external $\overline{CAS}$ is the result of gating $\overline{CAS}$ internal to the chip. The internal $\overline{CAS}$ is inhibited until the occurrence of a delayed signal derived from $\overline{RAS}$. Therefore, $\overline{CAS}$ can be activated as soon as the requirement for the row address hold time (tRAH) has been satisfied and the address inputs have been changed from row-to-column. The column address set up time (tASC) can be assumed to be zero for all dynamic RAMs (See Figure 1).

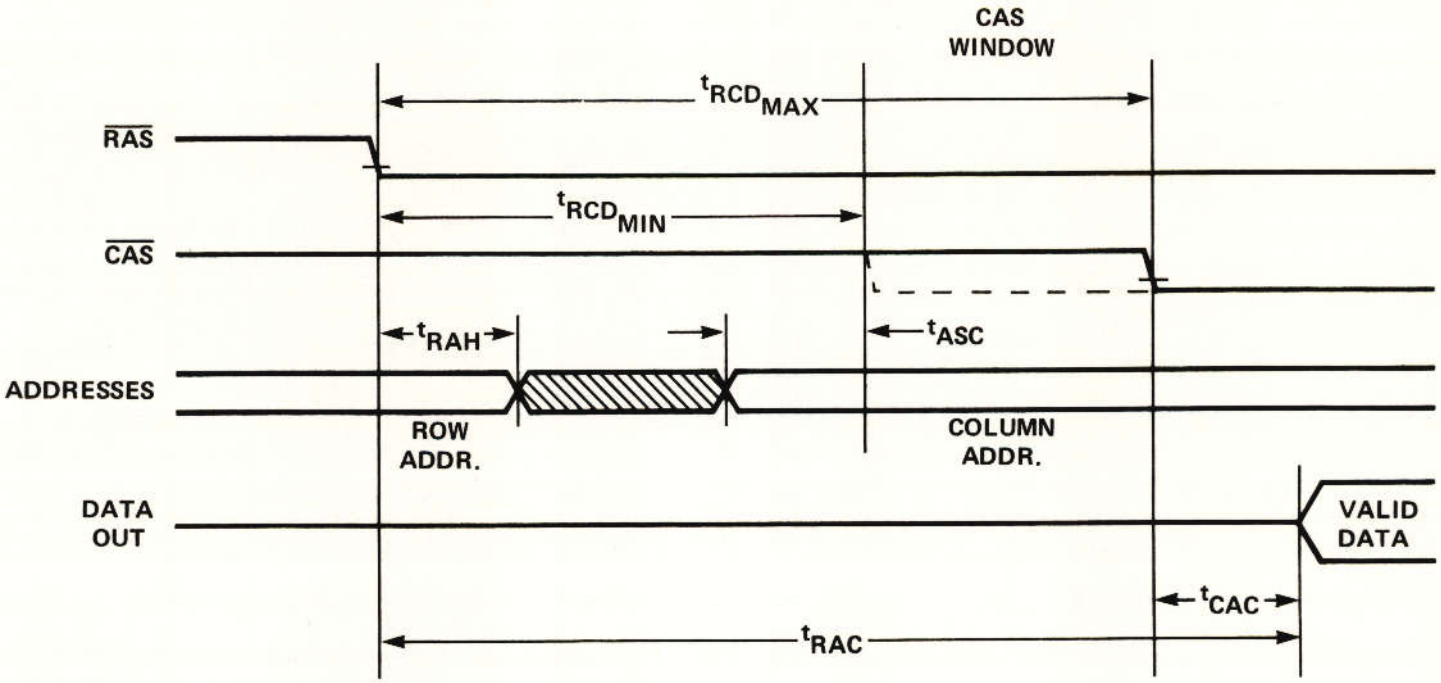


Figure 1 Dynamic ram access time parameters

Z80A/Z80 - CPU TIMING CONSIDERATIONS

The Z80A/Z80 CPU is uniquely designed to allow efficient and effective interface with dynamic RAM memories. Figures 2 through 7 identify the timing for CPU data, address and control signals associated with memory interface for the Z80A and Z80. The opcode fetch, with its associated refresh cycle, will represent the worst case memory access, requiring data to be returned to the CPU in the first two T states. Memory read and write cycles have relaxed timing requirements as indicated in Figures 4 through 7. This will require memories with access times of 250ns or less for the Z80A and 400ns or less for the Z80. These numbers, however, do not take into consideration the propagation delays through any buffer logic added.

Notice that addresses are stable well before $\overline{MREQ}$ goes active, giving sufficient time for address decode logic to settle. The main concern, therefore, is propagation delay from $\overline{MREQ}$ to $\overline{RAS}$. This should be kept to a minimum since it will directly affect access time.

From Figure 6 it can be seen that write ($\overline{WR}$) goes active on the trailing edge of T2. The CPU, therefore, usually performs a read-modify-write cycle. ($\overline{CAS}$ before $\overline{WR}$) To utilize the early write cycle ($\overline{WR}$ active before $\overline{CAS}$) and allow 16K systems to tie their inputs and outputs together, the read line ($\overline{RD}$) from the CPU can be inverted and used instead of $\overline{WR}$. This requires, however, that write data be valid before $\overline{CAS}$.

From Figure 3 it can be seen that the minimum high time for $\overline{MREQ}$ between opcode fetch and refresh cycles is 100 ns for the Z80A. For systems that use $\overline{MREQ}$ to generate $\overline{RAS}$ this is not sufficient to satisfy $\overline{RAS}$ precharge time requirements. However as will be shown in the design example, relatively simply logic can be used to extend $\overline{RAS}$ high time between these cycles.

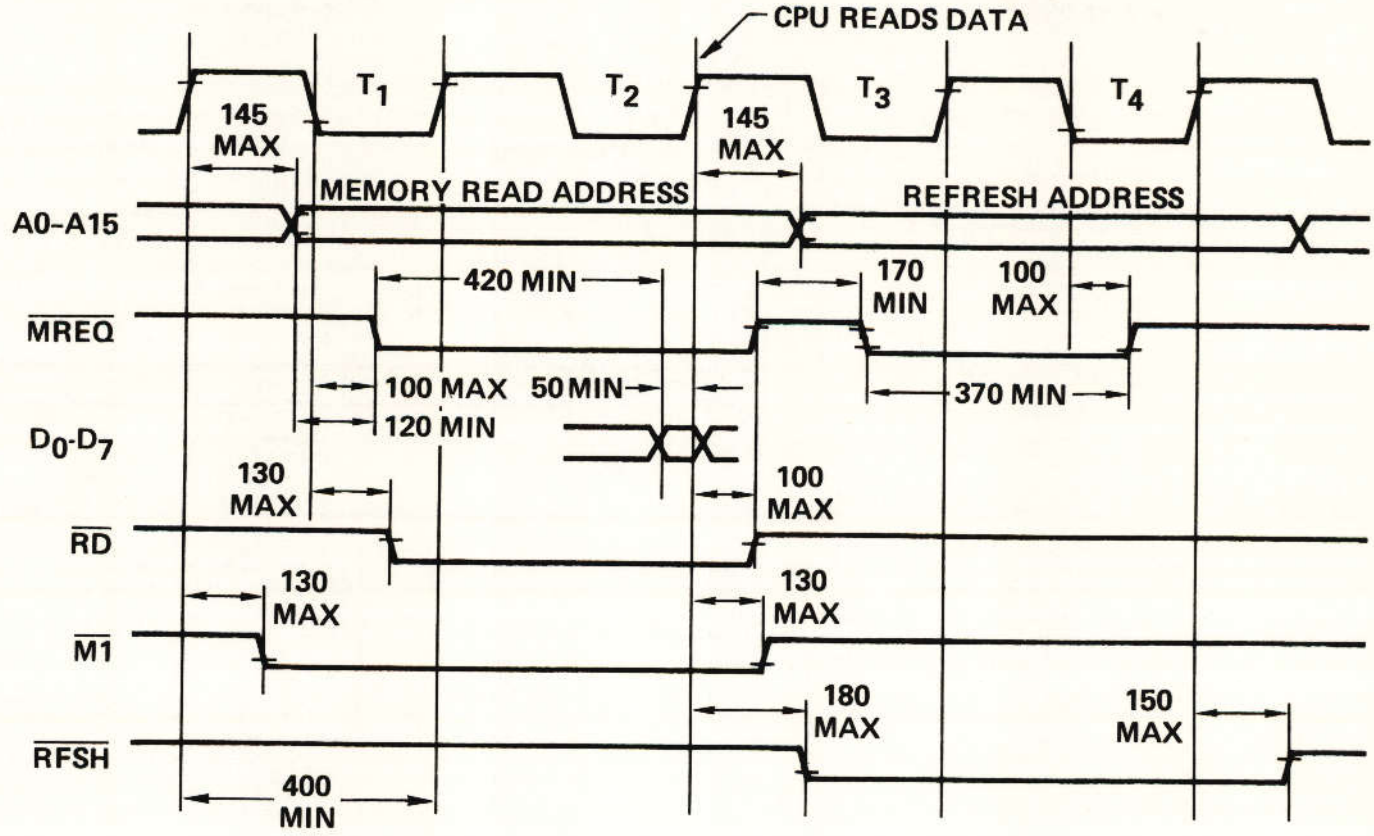
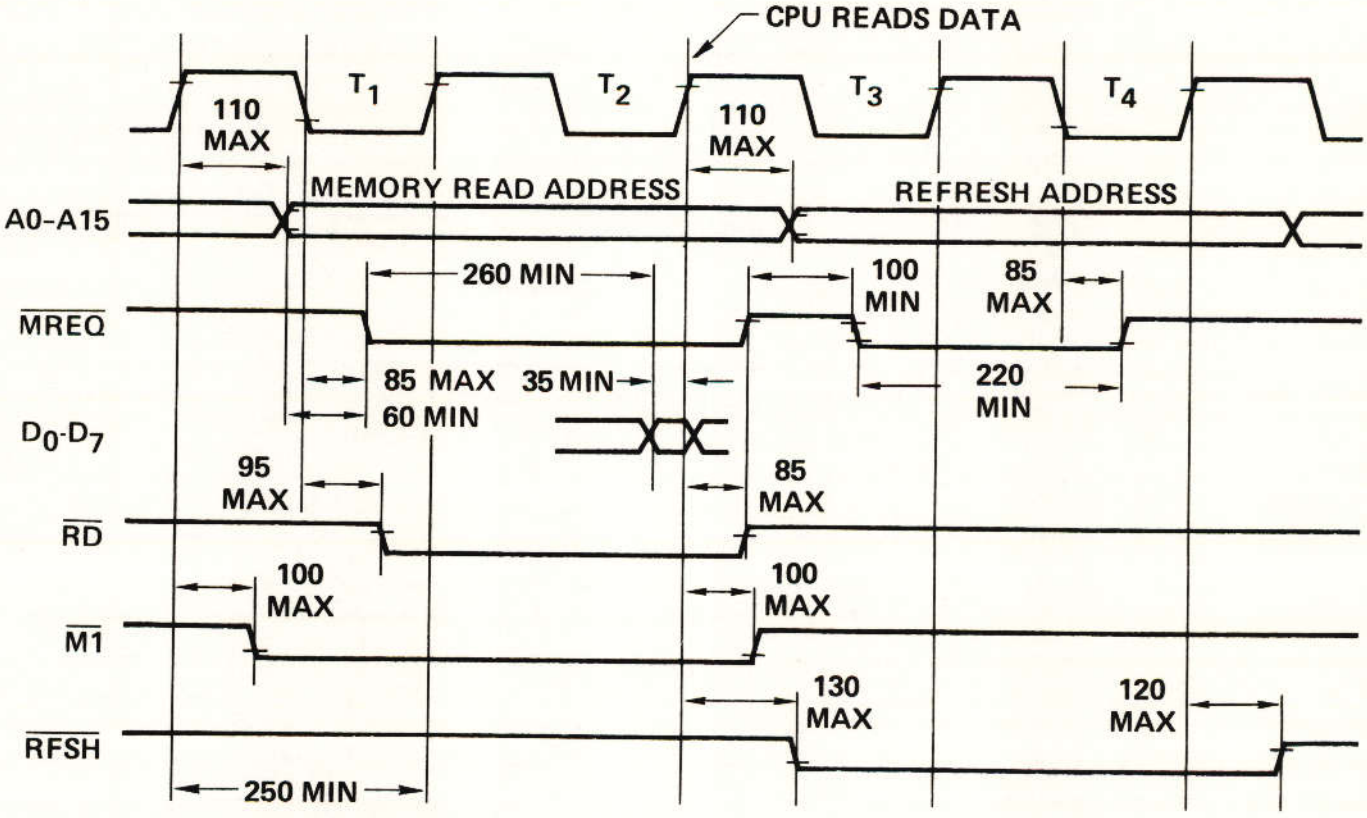


Figure 2 Z80-CPU op code fetch cycle timing at 2.5 MHz clock



NOTE: ALL TIMING IN ns

Figure 3 Z80A-CPU op code fetch cycle timing at 4 MHz clock

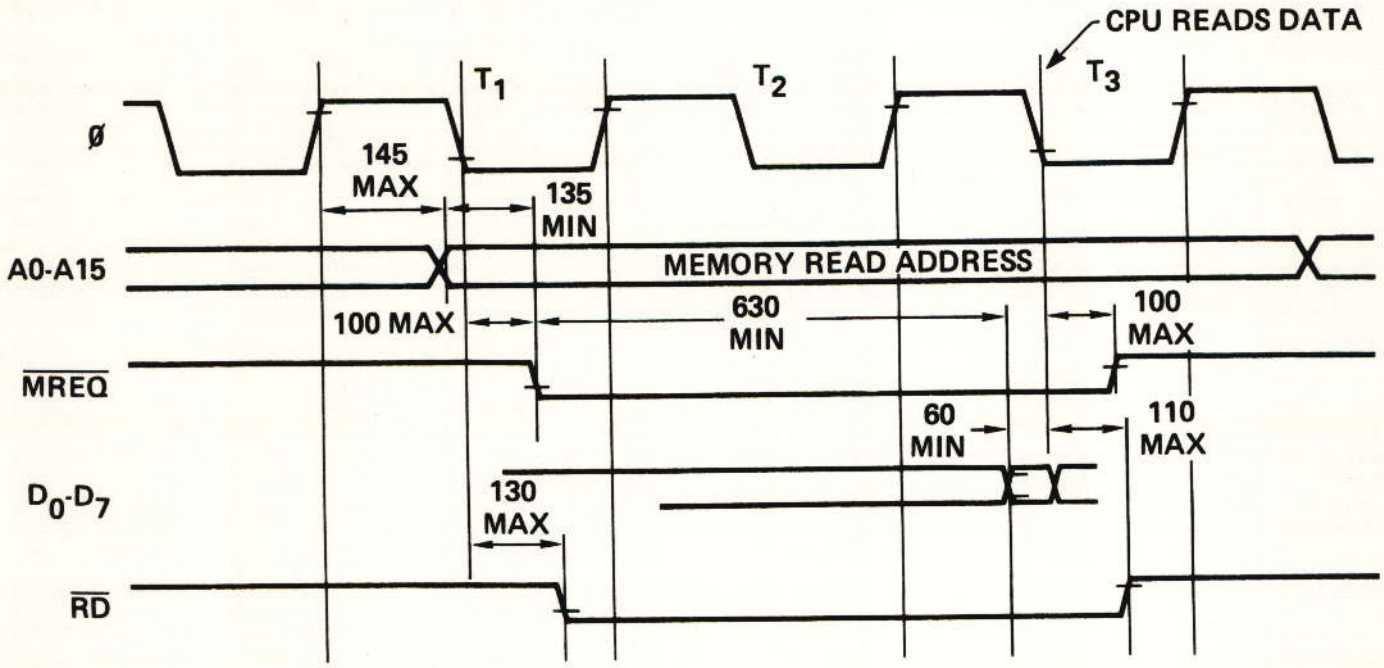
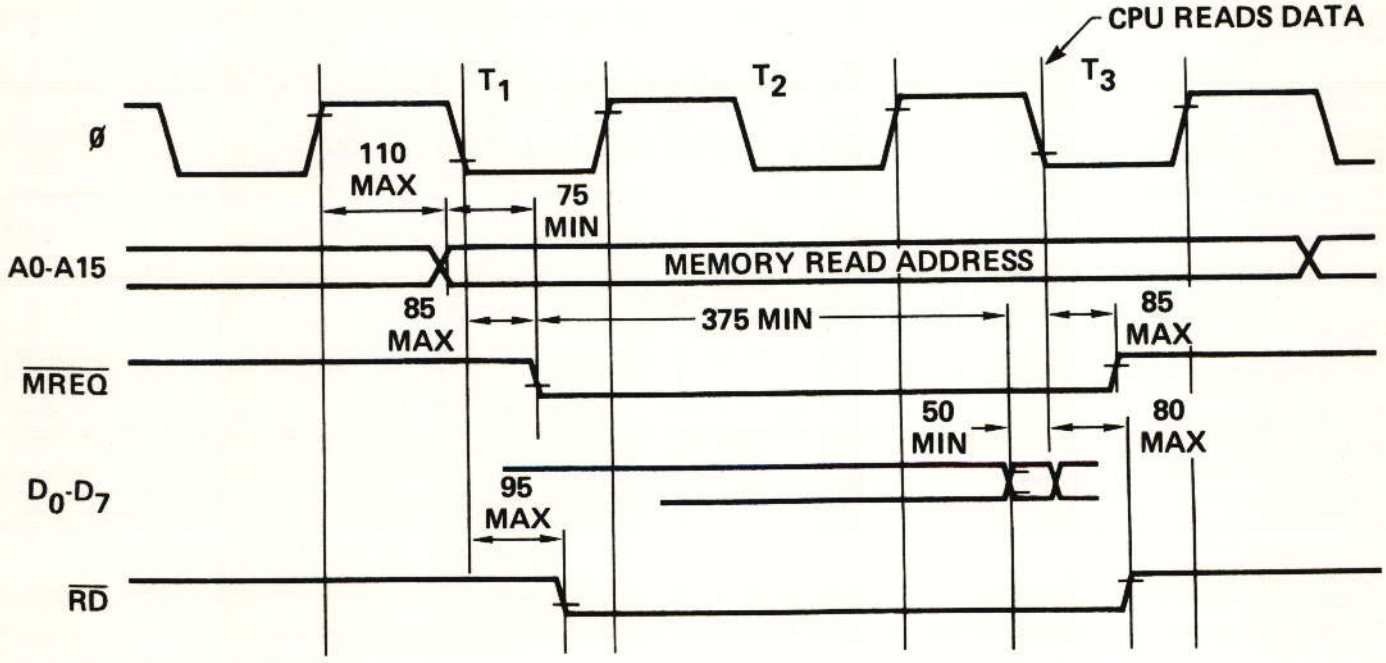


Figure 4 Z80-CPU read cycle timing at 2.5 MHz clock



NOTE: ALL TIMING IN ns

Figure 5 Z80A-CPU read cycle timing at 4 MHz clock

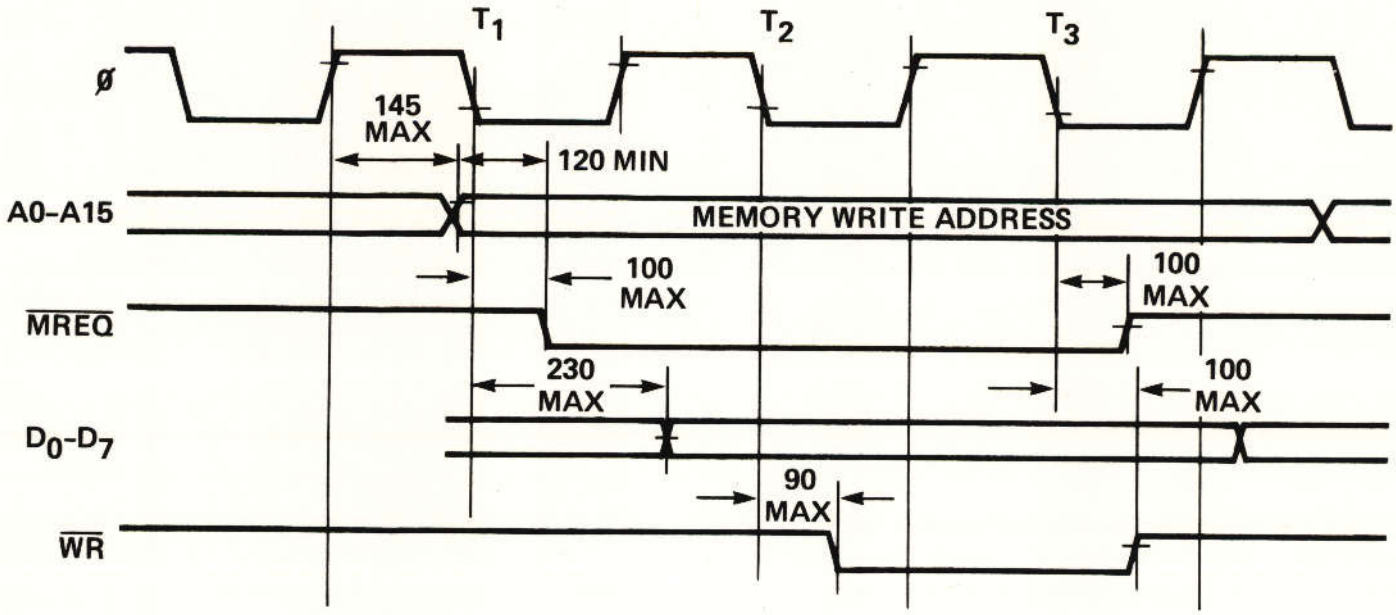
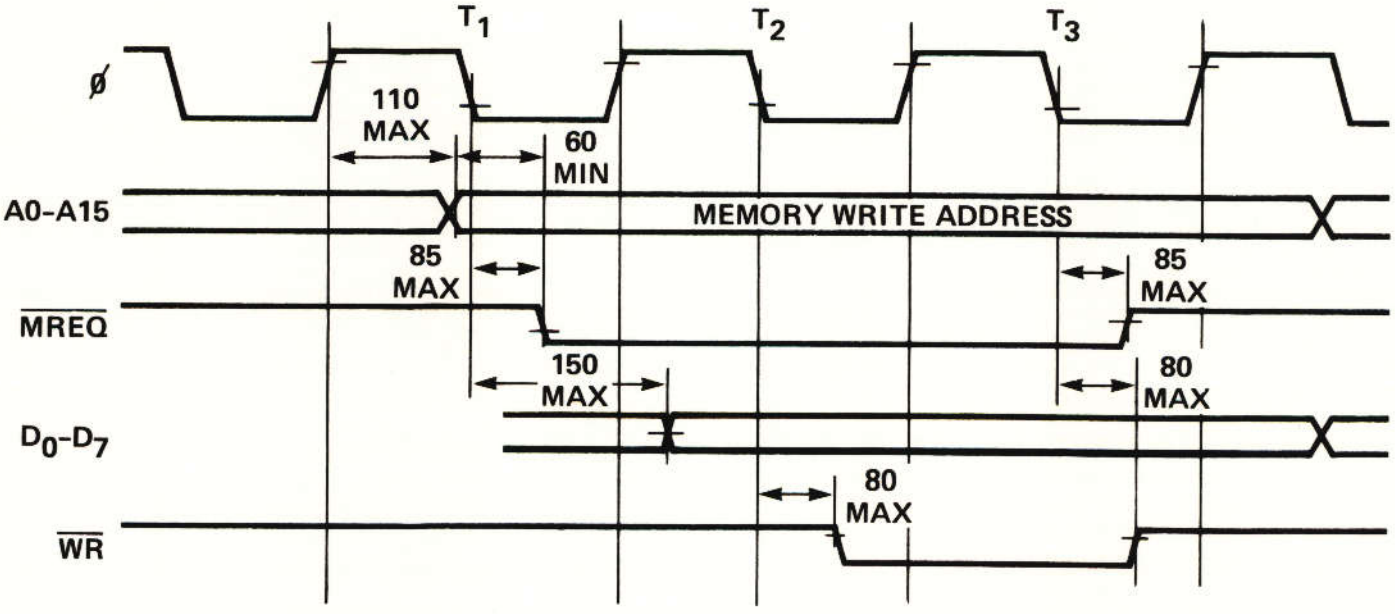


Figure 6 Z80-CPU write cycle timing at 2.5 MHz clock



NOTE: ALL TIMING IN ns

Figure 7 Z80A-CPU write cycle timing at 4 MHz clock

MEMORY CYCLE SELECTION

Selection of an operating mode is controlled by a combination of $\overline{CAS}$ and $\overline{WRITE}$ while $\overline{RAS}$ is active. The available modes in most 4K and 16K RAMS are a read cycle, a write cycle, a read-write cycle and a read-modify-write cycle. For some of the newer 4K devices and the 16K device another type of cycle known as page mode allows for faster access time by keeping the same row address and strobing successive column addresses onto the chip.

The read-modify-write cycle can be accomplished in less time than a read cycle followed by a write cycle because the addresses do not change in between. It is, therefore, possible to generate the write strobe as soon as the data modification is complete. In other words, data is read from a cell, modified and then rewritten in its modified form into the same cell. In constrast, a read-write cycle does not require data to be valid at the output before the write operation is started.

In a write cycle, if the $\overline{WRITE}$ input is brought low before $\overline{CAS}$ (early write) the data is strobed in by $\overline{CAS}$. In a delayed write cycle, the $\overline{WRITE}$ line goes low after $\overline{CAS}$ and data is strobed in with $\overline{WRITE}$.

DYNAMIC RAM MEMORY ORGANIZATION

Careful attention must be given to dynamic RAM memory array layout. Page decoding, power line routing and filtering, noise suppression and generation, buffer drive requirements and system upgrading are all important considerations during the design phase.

If a memory array consisting of 4K devices exceeds 4K bytes (one page), it will be necessary to configure multiple rows. Each row, or page, is selected by decoding address lines A12-A15. If the system is intended to be upgraded with 16K devices, the chip select line (CS) should not be used for device selection. Instead, $\overline{RAS}$ should be gated to the selected 4K bank with $\overline{CAS}$ being applied to all devices. (Chips that receive $\overline{CAS}$ but no $\overline{RAS}$ will be unselected.) The CS line should be distributed to all devices and tied to ground. It can then be used as the 7th address line when upgrading to 16K RAMS.

The $\overline{CAS}$ line is used to control the output buffer in a configuration where the outputs are or-tied. If true data is still available from a previous cycle (assuming latched output 4K RAMS), then $\overline{CAS}$ deselects these devices if they are not being accessed during the current cycle. Note also that if $\overline{RAS}$ is inactive and $\overline{CAS}$ active, the only function that is performed is to change any true outputs to the high inpedance state. Figure 8 shows the logic for one data bit in an 8K byte system utilizing two banks of 4K RAM devices.

The absence of an output latch on most 16K RAMS can allow for simplification in system design. Unlike the latched 4K devices which need an extra cycle to clear the latch, the 16K non-latched device maintains data valid only during the time the $\overline{CAS}$ clock is active. Each memory cycle, therefore, can be maintained as an independent cycle, allowing the data input and output pin to be directly connected. This is assuming, however, that the write line goes true before $\overline{CAS}$ (early write mode).

All inputs on most dynamic RAMS are TTL compatible (on some 4K devices $\overline{RAS}$, $\overline{CAS}$ and the write line require a 2.7 volt minimum logic 1 level which will require a pull-up resistor on the TTL driver). These TTL inputs, however, do not source current, but instead present

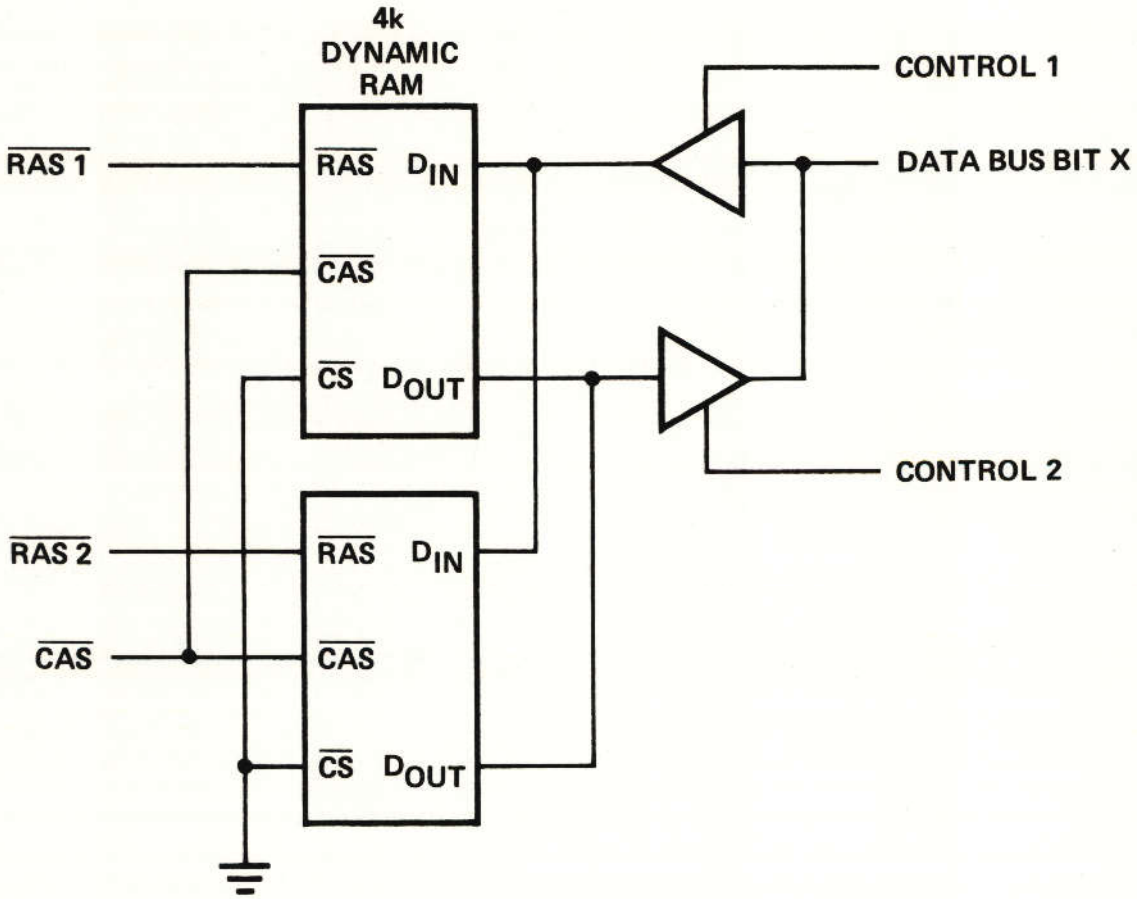


Figure 8 Partial memory configuration in 8k byte system

purely capacitive loads. This capacitance will vary between 5 and 10 pf on most 4K and 16K devices. With a large number of RAMS in a memory array capacitive loading becomes a consideration. A 16K byte memory array made up of 4K devices will present from 150 to 250 pf of input capacitance to the input buffers. Most TTL outputs are not specified above 50 pf. Therefore, a TTL driver must be used that can provide enough charging and discharging current to achieve the required voltage transition within the allotted time. A fairly accurate calculation can be made for determing the required drive current by using the standard relationship between the charging current i, the capacutance C, the voltage transition V, and the allotted time T:

$$i = C \frac{\Delta V}{\Delta T}$$

For example, if the worst case capacitance on an address line is 250pf, and it is required to change this address line within a 60ns period from zero volts to 3 volts, the driving current is:

$$i = 250 \times 10^{-12} \quad \frac{(3)}{60 \times 10^{-9}} \quad = \quad 12ma$$

The power consumption of dynamic RAMS which generally varies between 350mw to 1 watt depends on the state of the $\overline{RAS}$ and $\overline{CAS}$ clocks. The device draws minimum current when these clocks are inactive (standby mode). At each transition of the clocks, the device will draw current. This current corresponds to the precharging of these lines which represent large capacitance loads. During standby, the power consumption is usually less than 20 mw. Also because of this very low power dissipation when the clocks are turned off, the technique of decoding $\overline{RAS}$ to selected chips only, results in a sizeable decrease in power consumption (approximately 60% of all active power is due to $\overline{RAS}$ and only 40% is due to $\overline{CAS}$). Because the memory is dynamic, the power dissapation is a function of the rate of memory access and, therefore, operating frequency.

The resulting current spike which occurs when the $\overline{RAS}$

and $\overline{CAS}$ clocks go through their negative transitions is coupled onto the power supply busses causing noise throughout the system. To compensate for this noise, high- frequency ceramic bypass capacitors should be placed within the memory array. A good practice is to supply a .luf capacitor every other device between +12V and ground. Alternating between these capacitors, a.luf capacitor should be placed between -5V and ground. Decoupling on the +5V line to prevent noise from affecting TTL logic should consist of a .0luf capacitor every 4 or 5 devices. For low frequency decoupling a 10 uf tantalum capacitor between +12 and ground should be supplied every 16 devices with a 10 uf tantalum between -5V and ground every 32 devices.

The use of a multi-layer board with internal power and ground planes would be beneficial in a dynamic RAM system. However, proper routing of power lines on a two-sided card should provide satisfactory results. It has been found that bussing the +12 volt and ground lines both horizontally and vertically at every device will reduce noise and greatly improve RAM performance. The -5 and +5 volt lines need not be bussed in this fashion since they are less heavily loaded and are less likely to see current spikes.

Keeping the layout as small as possible and locating the address and data bus buffers as close to the array as possible will also reduce potential ringing and reflections.

Figure 9 represents a typical expandable RAM interface for a total memory capability of either 16K using 4K devices or 64K using 16K devices. The multiplexing of address lines is done by "wire-oring" 8T97 drivers and controlling the tri-state input for row to column switching. Since the minimum voltage on any RAM input is -1 volt, a small series resistor (about 30 ohms) is inserted on each RAM address line to surpass any undershoot that might occur. When using 4K RAMs, the lower section of the 74S139 decoder selects the desired 16K quadrant by decoding address lines A14 and A15. The upper section of the decoder selects the desired 4K bank in this quandrant by decoding address lines A12 and A13. When using 16K RAMs, the lower section of the decoder is not used and the upper section decodes the desired 16K quandrant with address lines A14 and A15. The latch on the upper address line is used to prevent potential spikes on the $\overline{RAS}$ lines as $\overline{MREQ}$ and the address lines change at the end of the cycle.

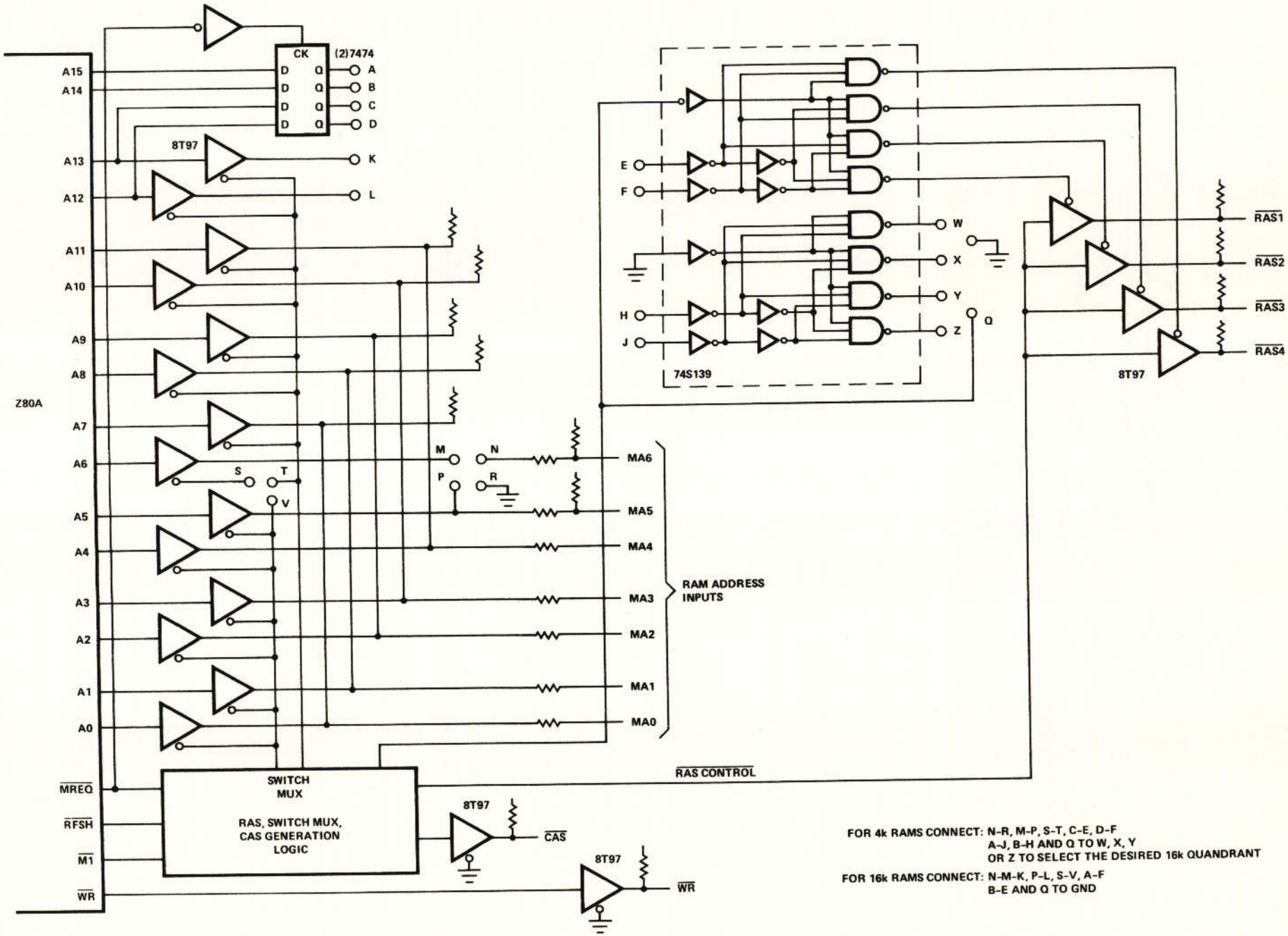
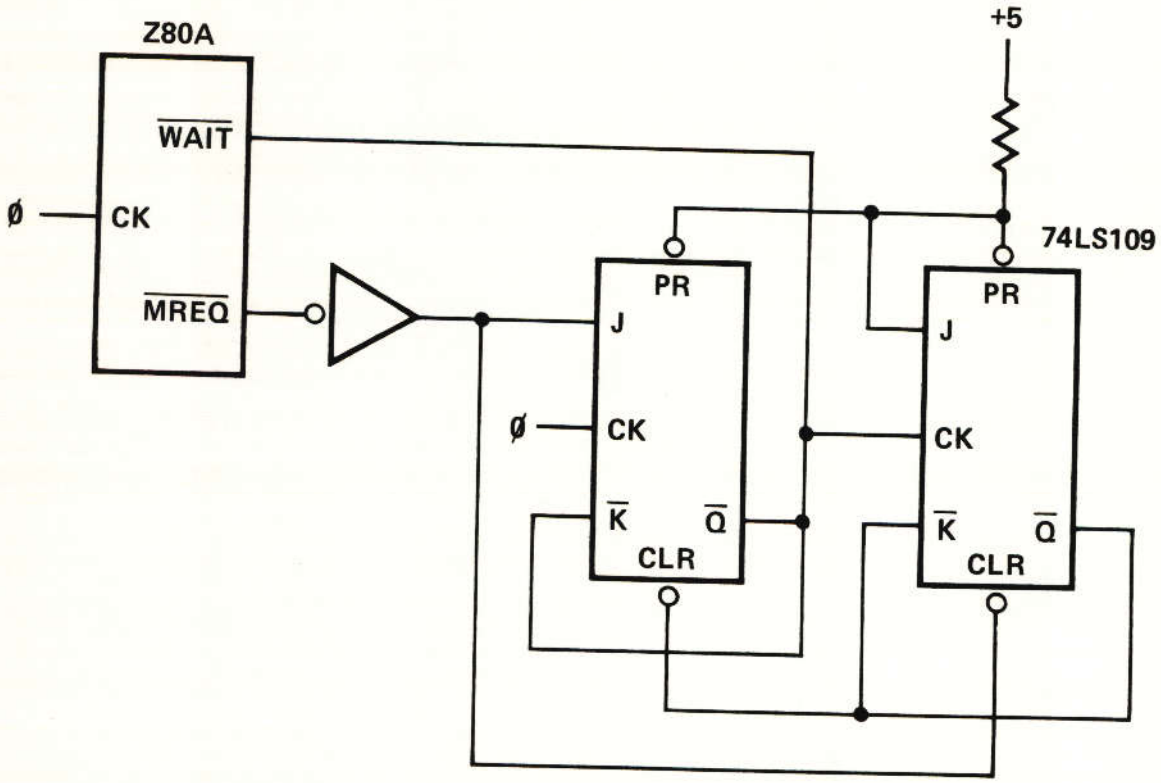


Figure 9 Z80A-16K/64K dynamic ram interface

The use of 8T97 drivers with an exterenal pull-up resistor, will insure proper logic level and capacitance drive capability. When using 4K devices, memory address line 6 (MA6) is not needed and tied to ground. (This is the chip select line on 4K RAMs.) When using 16K RAMs, this line is the 7th address line (A6 for row and A13 for column).

SLOW MEMORY INTERFACE

When working with memory devices with long access times (2708 EPROMS with a 450ns max access time, for example) it will be necessary to add wait states to Z80A timing. Figure 10 shows how a JK flip flop can be configured for adding one wait state (250ns) to each memory cycle. When using dynamic memories that have access times between 250 and 350ns, it is only necessary to add wait states for Op Code fetch cycles, since this cycle is the critical one in terms of memory access requirements. In this case, the logic in Figure 10 can be controlled by $\overline{M1}$ instead of $\overline{MREQ}$ to accomodate these memories.



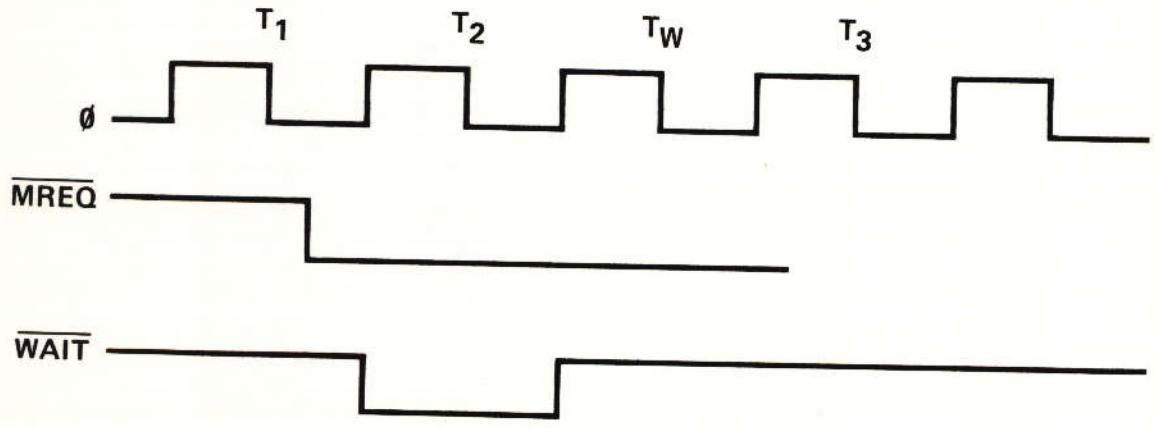


Figure 10 Adding one wait state to each memory cycle

DESIGN EXAMPLE

A typical design is presented to demonstrate a technique for dynamic RAM interface to the Z80A operating at 4MHz. Of the several approaches that could have been used for generating the timing signals needed for this interface, the trade offs for considering this approach consisted of the following:

1. Monostable-multivibrators could have been used to generate the time delays for the $\overline{MUX}$ switching and $\overline{CAS}$ signals, but one-shots are hard to adjust and are less reliable than other approaches.

2. The inherent delay in low power TTL gates could be used for this timing, but predictable timing intervals are hard to achieve at 4MHz.

3. A taped delay line produces very accurate timing signals but is less attractive from a cost standpoint.

The following synchronous technique was chosen for this design because it generates accurate signals with a minimum of logic complexity, and produces predictable results from system to system. The approach is to generate the CPU 4MHz clock from an 8MHz source. This 2Ø clock is then divided by 2 and used with the resulting Ø clock to generate the $\overline{MUX}$ switch and $\overline{CAS}$ signals after $\overline{RAS}$ has been generated from the fall of $\overline{MREQ}$.

Figure 11 is a schematic diagram of this interface. Figure 12 indicates the timing relationship involved.

The ROW Address Strobe ($\overline{RAS}$) is generated at the fall of $\overline{MREQ}$. On the next rising edge of the Ø clock 'A' Flip Flop is clocked to generate the signal used to switch the multiplexer from ROW addresses to Column addresses. The following falling edge of the 2Ø clock is used to generate the $\overline{CAS}$ signal (B flip flop). Flip Flop C is used to insure sufficient $\overline{RAS}$ precharge time, which must be taken into account since $\overline{MREQ}$ has a minimum high time of 100ns between Op Code fetch and refresh cycles and $\overline{MREQ}$, therefore, cannot be used to set $\overline{RAS}$ high. With $\overline{CAS}$ true, the trailing edge of $\overline{RAS}$ is clocked high with the Ø clock. This will extend the $\overline{RAS}$ high time to approximately 150ns.

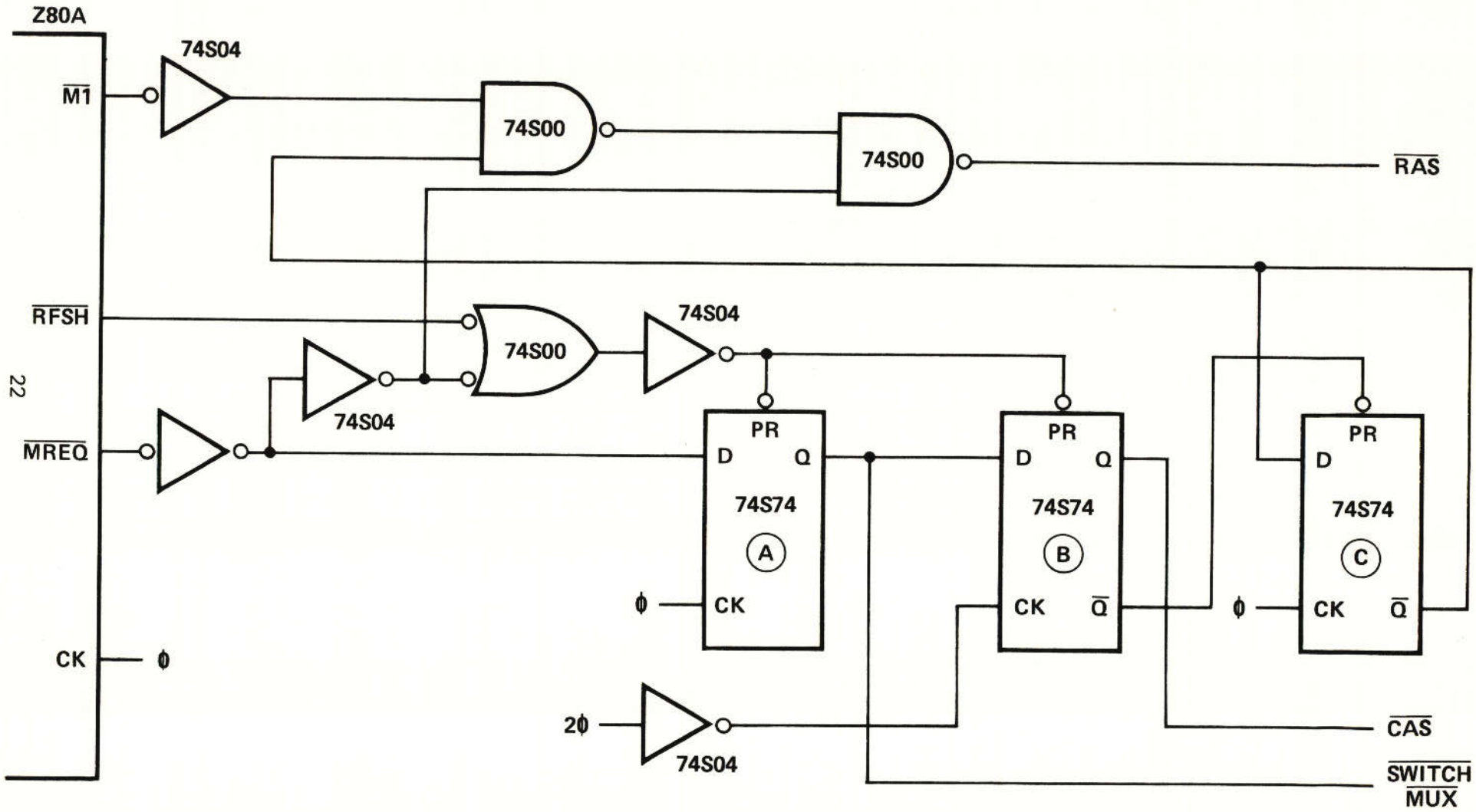


Figure 11 Z80A dynamic ram interface

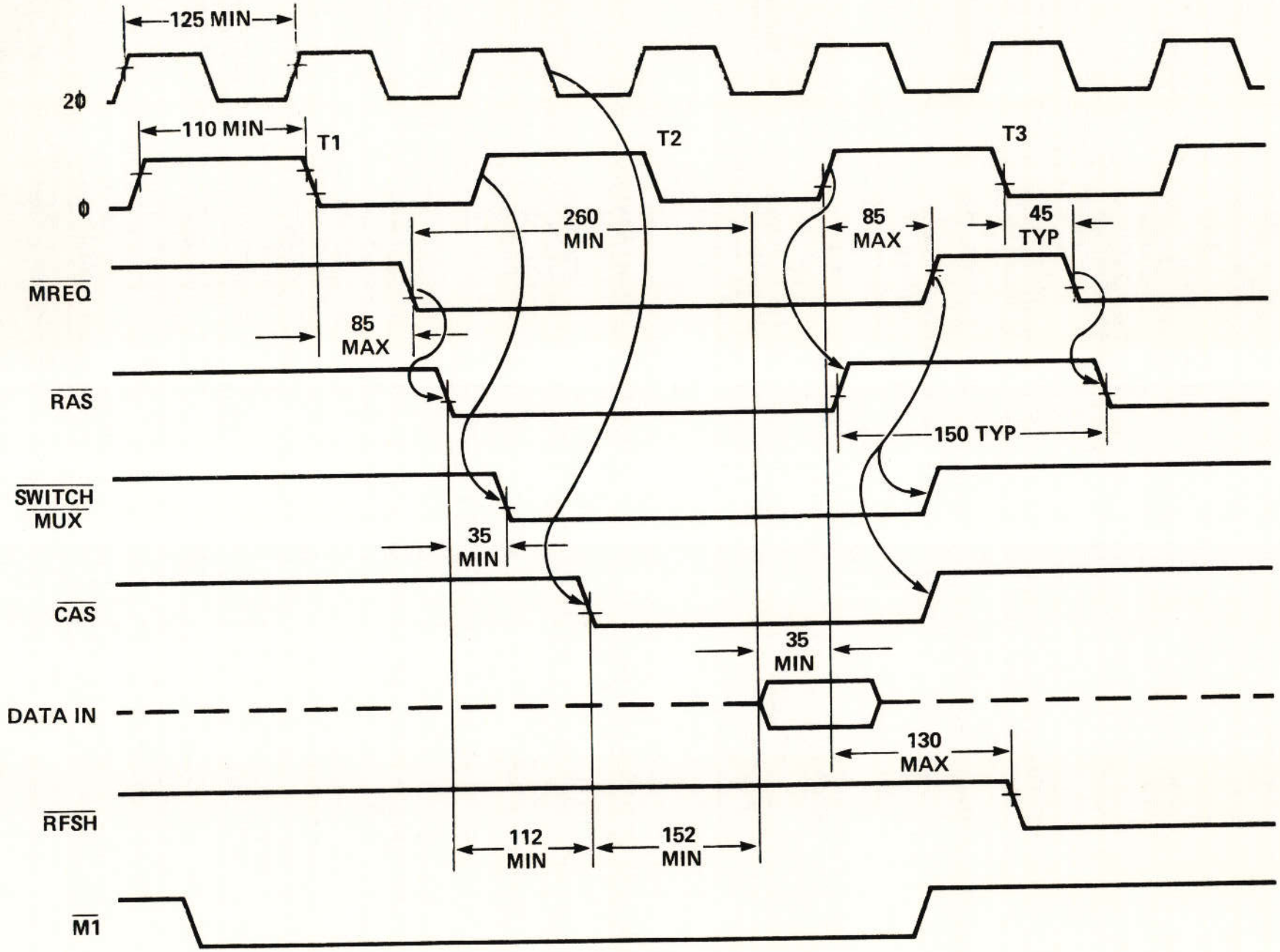


Figure 12 Z80A dynamic ram interface timing

This basic logic structure is configured into a microcomputer system and is seen in Figure 13. For simplicity, only the logic pertaining to the RAM interface is shown. Additional logic consisted of monitor software and a serial I/O interface to a CRT terminal.

Calculated timing parameters matched measured data quite accurately. Figures 14 through 19 indicate recordings taken during the Op Code fetch and refresh cycles at room temperature and at a Vcc of +5.0 volts. It can be seen that there is adequate allowance for variation in timing due to the temperature and voltage margins involved.

From Figure 18 it can be seen that the interval between the leading edge of $\overline{RAS}$ and the leading edge of the switch $\overline{MUX}$ signals is approximately 50ns. The calculated interval is 35ns minimum and is consistent with the ROW address hold time tRAH (see Z6116 Product Specification) of all RAMs that are access time compatible with the Z80A.

At the leading edge of the switch $\overline{MUX}$ signal, the RAM addresses are switched from ROW to Column addresses. Assuming the column address set up time (tASC) to be zero (consistent with most dynamic RAMs), the interval for address switching is approximately 70ns as confirmed from calculated and measured data (see Figures 12 and 18). Scope triggering records both Row and Column addresses which appear to be superimposed on a typical RAM address line as seen in Figure 16.

Since the $\overline{RAS}$ to $\overline{CAS}$ interval exceeds the tRCD max value of most access compatible RAMs, the RAM access time is measured from the leading edge of $\overline{CAS}$. RAMS with $\overline{CAS}$ access times of 150ns or greater should be compatible with this interface approach. If it is desired to keep the $\overline{RAS}$ to $\overline{CAS}$ interval within or closer to the tRCD max limit, a 4Ø clock could be applied to the clock input of FFB instead of the 2Ø clock. This would reduce the $\overline{RAS}$ to $\overline{CAS}$ interval to approximately 65ns.

The recordings also show the relation between $\overline{MREQ}$ and $\overline{RAS}$ high time between Op Code fetch and refresh cycles. The calculated value for $\overline{RAS}$ high time was 150ns while the measured value was approximately 170ns. This allows adequate $\overline{RAS}$ precharge time for all access compatible RAMs.

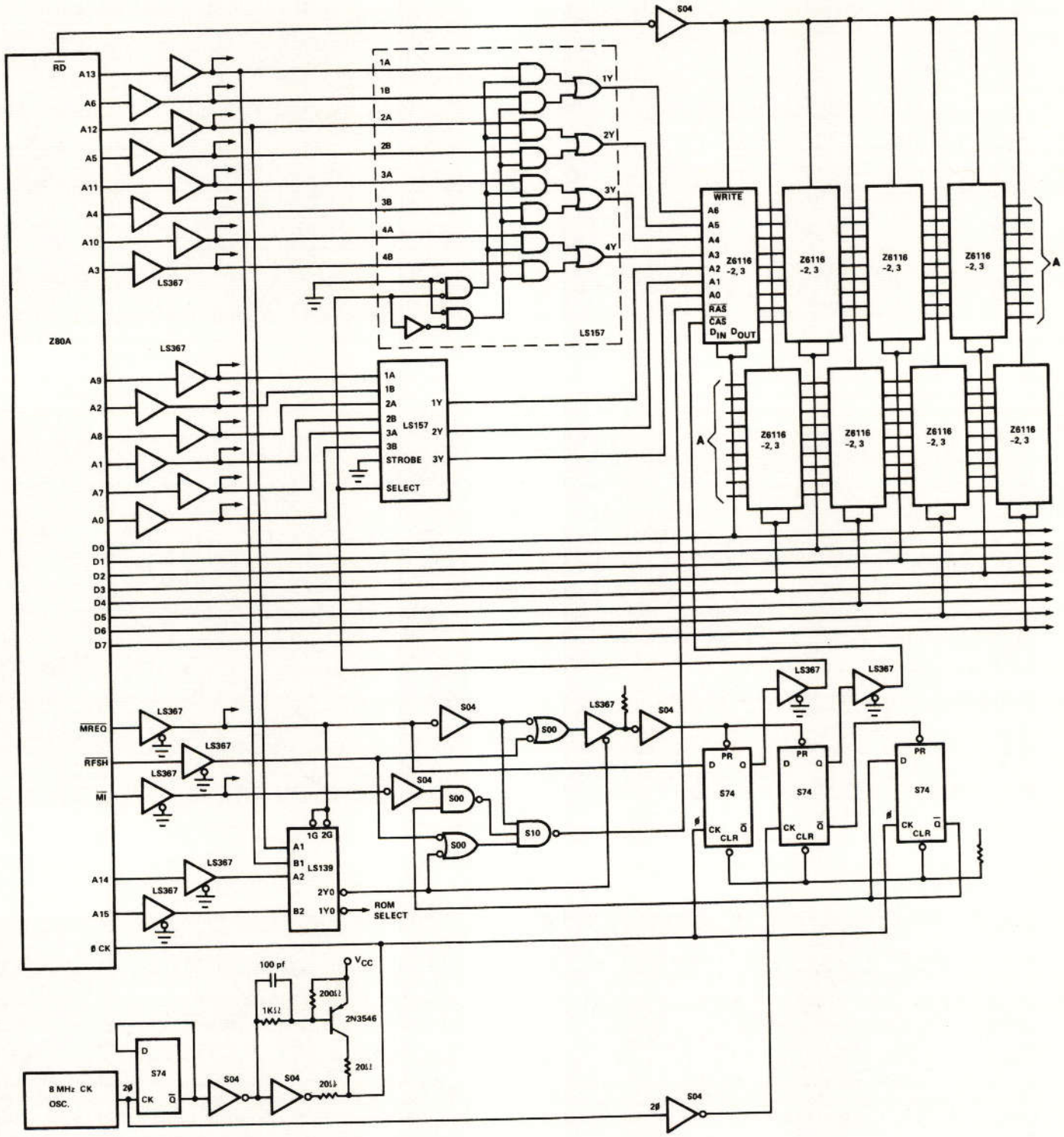


Figure 13 Z80A 16K ram interface

FIGURE 14

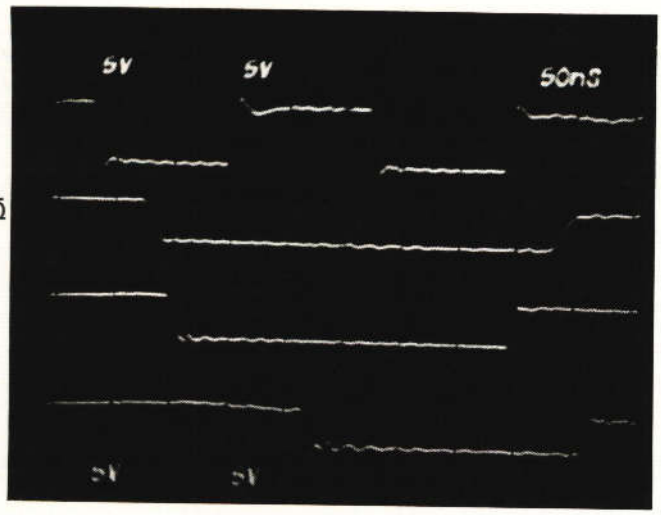


FIGURE 15

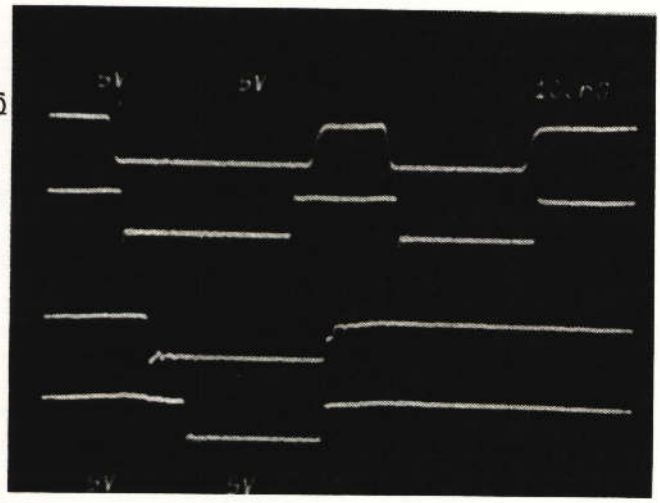


FIGURE 16

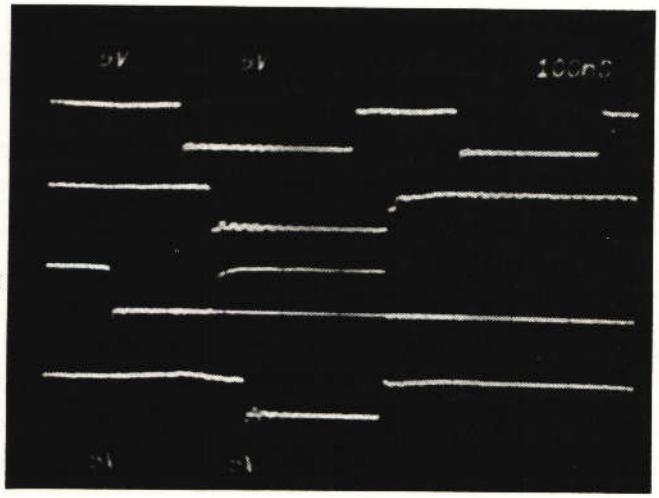


FIGURE 17

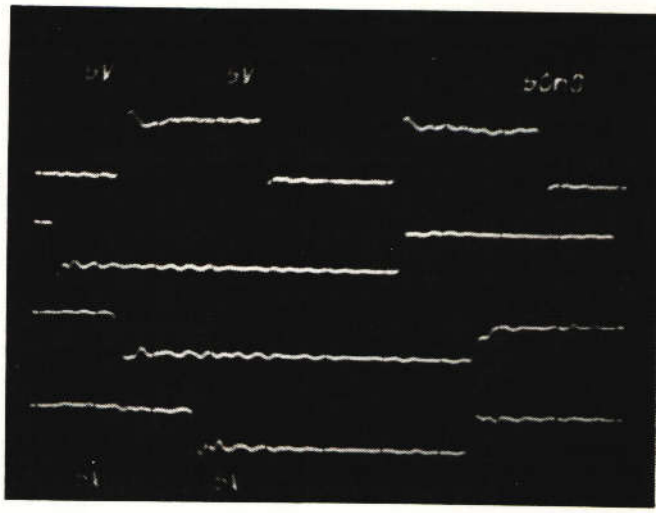


FIGURE 18

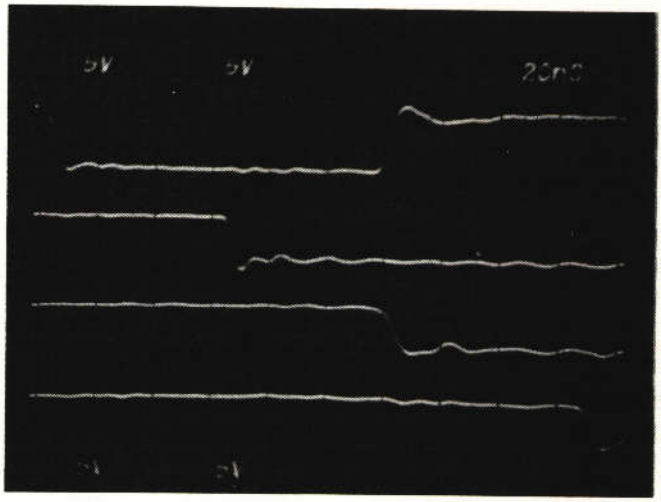
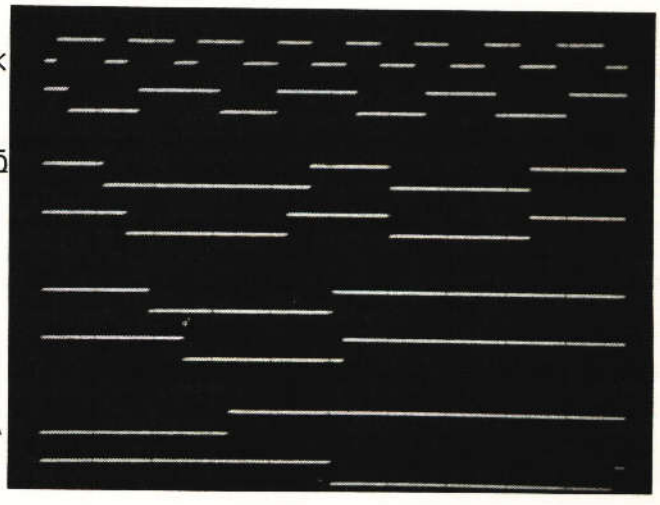


FIGURE 19



A composite of all the major control signals including one data line is seen in Figure 19. This recording, done with a logic analyzer shows the relative relation of these signals during the Op Code fetch and refresh cycles. Notice that during refresh only $\overline{RAS}$ is active with the switch mux and $\overline{CAS}$ signals disabled.

CONCLUSIONS

The Z80A has greatly simplified dynamic RAM interface. Internal logic operates totally transparent to CPU operation supplying refresh capability without the need for a refresh counter and its associated multiplexer. It has been shown that this interface can be configured with just 5 standard TTL gates to obtain synchronous generation of the $\overline{RAS}$, $\overline{CAS}$ and multiplexer switching signal. Additional attention must be given to the RAM layout which can have a dramatic affect on system performance. These devices tend to be noise generators as well as being noise sensitive but with proper filtering, power line routing and array organization, dependable performance can be achieved.

EUROPEAN HEAD QUARTERS:

Zilog (UK) Ltd.
Nicholson House,
Maidenhead, Berkshire.
UNITED KINGDOM
Tel. 0628-36131/2/3
Telex: 848609

USA:

Zilog Inc.
10460 Bubb Road,
Cupertino, Cal. 95014
Tel. (408) 446-4666
Telex: 910-338-7621

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Twx: 200491

FINLAND

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Ahertajantie 6D
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Twx: 122018

GERMANY

Kontron Elektronik GmbH
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Madrid (13)
also in Barcelona
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Twx: 10766

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Twx: 54070

UNITED KINGDOM

Cramer Electronics
16 Uxbridge Road
Ealing
London W5 2BP
Tel: 01 579 3001
Twx: 933592

Micropower Limited
Hampstead House
Basingstoke
Hants. RG21 1LG
Tel: (0256) 54121
Twx: 858572

Zilog

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